Amendments to the Specification:

Please amend the specification as follows:

Please replace paragraph starting at page 11, line 14, with the following rewritten paragraph:

FIGS. 1a-1b ~~is a drawing~~ are drawings showing an embodiment of the semiconductor device according to the present invention, where part FIG. 1(a) is a schematic plan view of the face on the bump formation side of an FCLSI, and part FIG. 1(b) is an enlarged plan view of portion A in FIG. 1 (a);

Please replace paragraph starting at page 11, line 21, with the following rewritten paragraph:

FIGS. 3a-3b [[shows]] show drawings schematically illustrating an example of the semiconductor chip constituting the FCLSI, where FIG. 3(a) and FIG. 3(b) are respectively a plan view and an example of the electrostatic protection circuit showing the configuration with the chip;

Please replace paragraph starting at page 12, line 2, with the following rewritten paragraph:

FIGS. 5a-5b ~~is a drawing~~ are drawings for describing the case when dummy bumps (DBPs) are concentrated in a corner part of the LSI, where FIG.5(a) and FIG.5(b) are respectively a schematic plan view showing the arrangement of the external connection bump electrodes, and an enlarged plan view showing also the connection with pads (PDs) on the chip of portion B in FIG.5(a);

Please replace paragraph starting at page 12, line 11, with the following rewritten paragraph:

FIGS. 7a-7b ~~is a drawing~~ are drawings showing an example of a conventional FCLSI, where FIG.7(a) is a plan view showing schematically the arrangement condition of the ball bumps on the side of face where ball bumps are formed, and FIG.7(b) is a partially enlarged

plan view including the connection wirings between the ball bumps in portion C in FIG.7(a) and the electrodes on the chip;

Please replace paragraph starting at page 12, line 18, with the following rewritten paragraph:

~~FIGS. 9a-9b is a drawing~~ FIGS. 9a-9c are drawings showing an example of a conventional BGA type LSI, where FIG.9(a) is a plan view of the back side where ball bumps are formed, and FIG.9(b) and FIG.9(c) are sectional views along line P3-P3' in FIG.9(a), which are examples when the electrodes of the semiconductor chip and the wiring conductors on the printed board are connected by a metal wire bonding and by a bump, respectively;

Please replace paragraph starting at page 12, line 25, with the following rewritten paragraph:

FIGS. 10a-10d ~~is a drawing~~ are drawings for describing the semiconductor chip disclosed in Japanese Patent Applications Laid Open, No. Hei 1-238148, where FIG.10(a) and FIG.10(b) are a plan view showing the arrangement of the bump electrodes and a sectional view of an important portion of the chip, respectively, and FIG.10(c) and FIG.10(d) are respectively schematic sectional views corresponding to the position along line P4-P4' in FIG.10(a) shown in the mounting order of the chip;